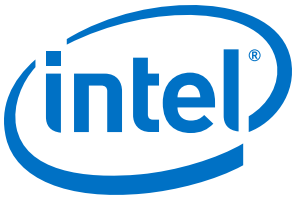

Other Transceiver IP Cores Product Release Notes

RN-1137
2016.10.31


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Contents

1 Other Transceiver IP Cores Product Release Notes

If a release note is not available for a specific IP core version, the IP core has no changes in that version. Information on the latest update releases is in the *Quartus Prime Design Suite Update Release Notes*.

Related Links

Quartus Prime Design Suite Update Release Notes

1.1 Transceiver PHY Reset Controller IP Core v15.1 Revision History

Table 1. v15.1 November 2015

Description	Impact

In ACDS 15.1, the Quartus Prime software includes a modification to Arria 10 designs using transceivers that controls and sequences `rx_analogreset` and `tx_analogreset` to transceiver channels. This new sequencing logic is inserted into the design during Quartus Prime compilation.
The Transceiver PHY Reset Controller IP core adds a new parameter (T_TX_ANALOGRESET) for Arria 10 devices. This change requires a modification to all instances of the Transceiver PHY Reset Controller IP core.
Configure the Transceiver PHY Reset Controller IP core with the following parameters for most designs:
`T_TX_ANALOGRESET (tx_analogreset duration) : 70000`
`R_RX_ANALOGRESET (rx_analogreset duration) : 70000`
`T_TX_DIGITALRESET (tx_digitalreset duration) : 70000`
These settings ensure that the new underlying reset sequencer logic has sufficient time to accept the reset inputs from the Transceiver PHY Reset Controller IP core.
	—

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

1.2 Transceiver PHY Reset Controller IP Core v14.1 Revision History

Table 2. v14.1 December 2014

Description	Impact
Added an optional port `pll_cal_busy`. To enable `pll_cal_busy` select **Enable pll_cal_busy input port** parameter under the **TX Channel** option in the Reset Controller IP Core parameter editor. If not enabled, then by default, this port is connected to 1'b0.	-

Related Links

- Arria 10 Transceiver PHY User Guide

- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

1.3 Transceiver PHY Reset Controller IP Core v14.0 Arria 10 Revision History

Table 3. v14.0 Arria 10 August 2014

Description	Impact
Upgraded to support the new IP Catalog. For more information about the IP Catalog, refer to *IP Catalog and Parameter Editor* in *Introduction to Altera IP Cores*.	-

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores

1.4 Transceiver PHY Reset Controller IP Core v13.0 Arria 10 Revision History

Table 4. v13.0 Arria 10 December 2013

Description	Impact
Initial release for Arria 10 devices.	-

Related Links

- Arria 10 Transceiver PHY User Guide
- Errata for Transceiver IP Cores in the Knowledge Base
- Introduction to Altera IP Cores