Lower Power Dissipation and Enhanced Design Flexibility

Altera Cyclone III and Cyclone IV FPGAs in Wireless Applications

Low power, high functionality, and low cost for pico/femto basestations

Cyclone III LS FPGAs for software defined radio

- Complete waveform integration for under 1/4 Watt
- Low static power for extended battery life
- 0.8-mm BGA packages (19x19 mm^2) minimize board space
- Cost optimized for the best value

Today's wireless applications call for the right mix of bandwidth, low power consumption, and flexibility to respond to new market requirements. With Altera® Cyclone® III FPGAs, you can take control of your wireless system specifications with an unprecedented combination of low power, high functionality, and low cost. And with Cyclone IV FPGAs, you get a device family with the lowest cost and power, as well as an integrated transceiver variant.

Design Challenges

Your next wireless design must increase bandwidth dramatically and incorporate new standards while keeping equipment cost and power consumption as low as possible. ASICs are notoriously risky when standards and market demands are changing. Digital signal processing (DSP) devices often carry a large thermal tax, or limit the number of channels you can support. You need a low-power, low-cost solution that delivers design flexibility with low risk.

Low-Power, Low-Cost Flexibility

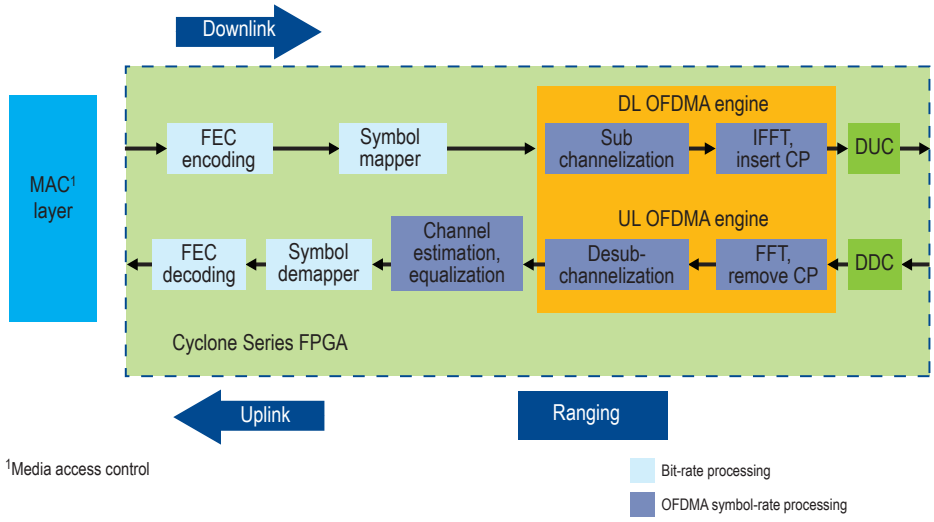
Because of their reprogrammability, low power, high functionality, and low cost, Cyclone III and Cyclone IV FPGAs enable a new class of wireless designs. Abundant 18x18 multipliers and on-chip memory allow you to implement low-power signal processing functions in a smaller footprint than ever before. Both device families are ideal for RF and channel cards in micro, pico, and femto basestations, remote radio heads, WiMAX customer premises equipment (CPE), and software-defined radio (SDR) applications, among many others. Intellectual property (IP) and tools from Altera and its wireless technology partners allow you to use pre-optimized software to save time and resources.

For extremely power-sensitive wireless applications, the Cyclone III LS FPGA features 200K logic elements for under ¼ Watt. You'll also decrease power dissipation for next-generation basestation equipment while gaining design flexibility for optimizing algorithms over the entire product life cycle. For transceiver applications, Cyclone IV GX FPGAs, with 3.125-Gbps transceivers, lower total system power and provide a flexible clocking structure for implementing multiple protocols.

Cyclone III and Cyclone IV FPGA Highlights

Highlighted Features	Benefits
Embedded memory	Up to 8.2 Mb of embedded RAM in Cyclone III FPGAs and up to 6.5 Mb of embedded RAM in Cyclone IV FPGAs, ideal for memory-intensive algorithms such as forward error correction (FEC)
DSP multipliers	Up to 396 embedded 18x18 multipliers in Cyclone III FPGAs and up to 360 embedded 18x18 multipliers in Cyclone IV FPGAs to implement DSP-intensive functions such as finite impulse response (FIR) or fast Fourier transform (FFT)
Low power	60-nm low-power (LP) process technology Power optimization features in the Quartus® II design software
Autocalibrating external memory interfaces	Easy implementation to support high performance of up to 400 Mbps with easy timing closure for DDR and DDR2
I/O bandwidth	Cyclone III and Cyclone IV FPGA: 668 Mbps QDR II memory interface performance, 400 Mbps DDR2 memory interface performance, and 840 Mbps LVDS I/O performance with dynamic phase alignment (DPA)

WiMAX Pico Basestation



Altera enables complete low-cost wireless solutions

- Altera and partner intellectual property (IP) cores, including FEC, FFT/IFFT, FIR, numerically controlled oscillator (NCO), and CIC functions, among others
- DSP Builder—automatically integrates Quartus II software and The MathWorks MATLAB and Simulink tool. A new capability, DSP Builder Advanced Blockset, facilitates timing-driven Simulink synthesis so you can achieve high-performance design implementations running at near-peak FPGA performance in a matter of minutes.
- Nios® II soft-core embedded processor
- Free Quartus II Web Edition software
- Low-cost development kits
- Application-specific reference designs
- White papers

In this WiMAX pico basestation design, the digital upconverter (DUC) and digital downconverter (DDC) use complex filter architectures including FIR and cascaded integrator-comb (CIC) filters. The downlink (DL) orthogonal frequency-division multiple access (OFDMA) symbol-rate processing includes the subchannelization, IFFT, and cyclic prefix (CP) insertion functions. The uplink (UL) OFDMA symbol-rate processing includes CP removal, FFT, desubchannelization, and channel estimation and equalization functions. The processing block utilization table illustrates resource usage for a WiMAX pico basestation design implemented in a Cyclone Series device.

The complete IF, OFDMA symbol-rate, and bit-rate processing can be implemented in a Cyclone series FPGA with under 2.5 Watts of power consumption. The abundant on-chip memory and high-speed multipliers in Cyclone III and Cyclone IV FPGAs provide a low-power, low-cost platform for implementing 3G and WiMAX basestation functionality.

Want to Dig Deeper?

For more information about how Cyclone III and Cyclone IV FPGAs, can help you meet your wireless design requirements, contact your Altera sales representative or FAE, or visit www.altera.com/wireless.

Picocell Basestation Processing Block Utilization

		Logic Elements (LEs)	Number of M9K Memory Blocks	18x18 Multipliers	Power Utilization (W)
IF Processing	DUC	2,704	50	30	0.4
	DDC	4,786	46	25	0.4
OFDMA Symbol-Rate Processing	DL OFDMA engine	4,176	33	4	0.25
	UL OFDMA engine	3,834	57	4	0.25
	Channel estimation and equalization	7,400	1	4	0.33
Bit-Rate Processing	Symbol mapper and demapper	1,404	3	0	0.1
	FEC (encoding and decoding)	18,511	26	0	0.6
	Total	**42,815**	**216**	**67**	**2.33**

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